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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/634,001	08/04/2003	Ming-Ching Chang	67,200-1107	5032

7590 09/21/2005

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EXAMINER	
GEORGE, PATRICIA ANN	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 09/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/634,001	CHANG ET AL.	
	Examiner	Art Unit	
	Patricia A. George	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08/04/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on ____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, lines 8 to 9, and claim 14, lines 9-11, the phrase "patterning the hardmask layer" is unclear because the subsequent "first ...RIE step", also patterns the hardmask. The steps involving the patterning of the hardmask are unclear. Does the applicant intend to cite both the patterning of a photoresist layer on top of the hardmask and then the use of that pattern for the first reactive ion etch step?

In claim 1 (lines 17-19) and claim 14 (lines 19-20) the term "at least one of" should cite –at least one member selected from the group consisting of— in order to have proper Markush group terminology. Alternatively, the term –or— can be used instead of "and". The claim reads....which includes selecting both the source and bias power to be lowered.

In claim 1, line 20, the term "the exposed gate dielectric" lacks proper antecedent basis because the previous step does not cite to expose the gate dielectric.

In claim 9 (lines 2-3) and claim 19 (lines 2-3) the term "combination of one of" should cite –at least one member selected from the group consisting of— in order to have proper Markush group terminology.

Claims 2-8, 10-13, 15-18, and 20-23 fail to cure the indefiniteness of their base claim and are therefore also rejected.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 2, 4-9, 11-12, 14-19, and 21-22 rejected under 35 U.S.C. 103(a) as being unpatentable over Lee of USPN 5,665,203 in view of Pan et al of USPN 6,656,832.

As for independent claims 1 and 14, Lee et al. discloses a method of Reactive Ion Etching (RIE) of polysilicon gate structures for vertical sidewalls (col. 1, l. 6-7) that obtains accurate pattern transfer (col.6, l.39-40). Lee teaches a gate dielectric (fig. 4, 22 and col.3, l.35) formed over a silicon substrate (fig. 4, 21 or col.3, l.32) and a polysilicon layer (fig.4, 23 and col.3, l.36) formed over the gate dielectric; providing a

hardmask layer (fig.4, 52 and col.4, l.11-12) over the polysilicon layer; using a photo resist layer (col.3, l.50) to pattern the hardmask layer for forming parallel N and P type polysilicon gates (fig.5, 12 &13) written on gate electrodes. Lee discloses a method of RIE that has three steps (col.4, l.28) and a typical over etch (col.4, l.57), which is written on four RIE etch steps. Lee discloses the first RIE step etches through any oxide that is formed on the polysilicon layer (col.4, l.32-32), written on etching on hardmask layer to expose the polysilicon layer. Lee discloses the second RIE step etches through all but 20 nm of polysilicon which is written on to etch through a first thickness portion of the polysilicon layer. Lee discloses a third RIE step that has a polysilicon to silicon oxide selectivity (col.4, l.52), which is written on etching through the second thickness portion of the polysilicon layer. Lee also discloses the bias power is at 50 watts (col.4, l.54), a lower setting than use for the second RIE step, 200 watts (col.4, l.41) (as in claims 5 and 15). Lee discloses an over etch that follows the third RIE step that is timed to reach the gate oxide (col.4, l.59), which is written on a fourth RIE etch process to etch through a remaining thickness of the polysilicon layer.

Lee does not disclose plasma treating the exposed gate dielectric and polysilicon layer in-situ wherein the plasma is formed essentially from an inert source gas to neutralize an electrical charge imbalance, as in claims 1 and 14.

Pan teaches argon plasma treatment (col.3, l.25) of sidewalls and floors (col.3, l.23) formed in a patterned conductor layer (col.3, l.25) that were formed with electrical properties (col.3, l.26-28), with a range of 450 to 0 Watts RF bias, as in claims 1, 2, 6, and 16.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to include the controlled plasma treatment process, of Pan, with the method of Reactive Ion Etching vertical sidewalls of polysilicon gate structures, of Lee, because Pan teaches reduction in current leakage and more stable normalized resistance which results in fewer electrical defects, a higher yield, and cost savings.

As for claim 4, Lee illustrates in figure 2 (parts 28 and 30) that the polysilicon layer includes both n and p doped regions used to form doped polysilicon gate electrodes shown in parallel (col.3, l.42-46).

As for claims 7-8 and 17-18, Lee discloses the third and fourth RIEs are carried out with 45 sccm of HBr, 3 sccm (70%) of He, and 30% O2, which as claimed, is a chlorine-free etching chemistry comprising HBr and oxygen.

As for claims 9 and 19, Lee discloses a combination of HBr/Cl.sub.2/O.sub.2 in the first and second etch steps (col.4, l.39-40 and c.4, l.46-50).

As for claims 11 and 21, Lee discloses the gate dielectric is thermally grown SiO.sub.2 (col.3, l.33-34). .

As for claims 12 and 22, Lee discloses the hardmask layer is LTO (col.3, l53 and 55).

As for claims 5 and 15, Lee is silent on the topic of RF source power and does not reference it, including the lowering the source power in the third step.

Claim Rejections - 35 USC § 103

Claims 3, 10, 13, 20, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee and Pan (see discussion above) in further view of Lill et al. of USPN 6,284,665.

Lee does discuss the benefits of self-bias (which is written on zero bias power) and the benefit of reducing etching bias with an over etch step, but never explicitly discloses the RF bias is set to zero. Lee is also completely silent about RF frequency, or that it is adjustably decoupled.

Lill et al. further teaches typical process conditions for RIE of polysilicon selectively to silicon nitride. Lill teaches the use of no-bias power to minimize the amount of self-bias on the substrate (col.10, l.15-30), as in claims 3, 13, and 23. Lill also teaches the RF bias power is supplied at the claimed frequency of greater than about 1 MHz (col.8, l.4) and in figure 2 Lill illustrates the RF bias power and is adjustably decoupled (col.10, l.4) from the RF source power, as in claims 10 and 20.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to use the typical process conditions for RIE of polysilicon selectively to silicon nitride, of Lill, when using the method of RIE for polysilicon gate structures, of Lee and Pan, because Lill teaches they are typical for RIE of polysilicon.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Referring to the reduction of plasma charge-induced damage in micro-fabricated devices see USPN 6,440,756.

Referring to a hardmask layer of silicon oxide, silicon nitride, and silicon oxynitride: USPN 6583063, USPN 6566264, and USPN 6194323.

Referring to zero RF power during RIE: USPN 5679606, USPN 6759337, USPN 6184158, USPN 6251792, and USPN 6143625.

Referring to RF bias power supplied at a frequency greater that 1 MHz: Table 1: Typical characteristics of low pressure plasmas used for reactive ion etching on page 198 of The Handbook of Plasma Processing Technology - Fundamentals, Etching, Deposition, and Surface Interactions, edited by Rossnagel et al, shows typical RF bias power is supplied at a frequency of 10 kHz – 27 MHz, also see USPN 6372654.

Referring to gate dielectrics of thermally grown SiO.sub.2, binary oxides, and binary lanthanum oxides, having a dielectric constant of greater than about 20: SN 10/ 038410, and USPN 6620713.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patricia A. George whose telephone number is (571)272-5955. The examiner can normally be reached on weekdays between 7:00am and 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on (571)272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Patricia A George
Examiner
Art Unit 1765

PAG
08/05

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, (lines 8 to 9) and claim 14 (lines 9-11) the phrase "patterning the hardmask layer" is unclear because the subsequent "first ...RIE step", also patterns the hardmask. The steps involving the patterning of the hardmask are unclear. Does the applicant intend to cite both the patterning of a photoresist layer on top of the hardmask and then the use of that pattern for the first reactive ion etch step?

In claim 1 (lines 17-19) and claim 14 (lines 19-20) the term "at least one of" should cite –at least one member selected from the group consisting of— in order to have proper Markush group terminology. Alternatively, the term –or— can be used instead of "and". The claim now cites to select both the source and bias power to be lowered because of the term "and".

In claim1, line 20, the term "the exposed gate dielectric" lacks proper antecedent basis because the previous step does not cite to expose the gate dielectric.

In claim 1, line 21, the term " formed essentially from" is unclear. May other gasses be combined with the inert gas? Or is only inert gas present? The specification and prior art lack a clear, explicit def. For "plasma source gas."

In claim 9 (lines 2-3) and claim 19 (lines 2-3) the term "combination of one of" should cite –at least one member selected from the group consisting of— in order to have proper Markush group terminology.

Claims 2-8, 10-13, 15-18, 20-23 fail to cure the indefinitness of their base claim, and are therefore also rejected.

Allowable Subject Matter

Claims 1-23 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph set forth in this Office action.

Conclusion

This application for a multi-step gate etch with in-situ inert plasma treatment is in condition for allowance except for the rejection(s) set forth in this Office action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patricia A. George whose telephone number is (571)272-5955. The examiner can normally be reached on Monday – Friday from 8:00am - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on (571)272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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